This listing of claims will replace all prior versions, and listings, of claims in the application:

In the claims

Claim 1 (previously presented): A programmable logic device (PLD), comprising:

a plurality of logic elements (LE's) arranged in an array;

a signal routing architecture including a plurality of signal routing lines to route signals among the LE's; and

a plurality of signal drivers along each of the signal routing lines,

wherein

for each of the signal routing lines,

the drivers along that signal routing line are spaced along that signal routing line;

for each of a first set of at least some of the signal routing lines,

that signal routing line is substantially interrupted by an interface region such that a partial signal routing line is formed for that signal routing line between the interface region and a driver along that signal routing line from the interface region; and

the PLD further comprises an input driver configured to drive from the interface region along the partial signal routing line formed for that signal routing line.

Claim 2 (original): The PLD of claim 1, wherein:

for each of the first set of at least some of the signal routing lines, the input driver configured to drive from the interface region along the partial signal routing lines for that signal routing line is characterized by a size that corresponds to a distance from the interface driver to the driver on the signal routing line closest to the interface region along the signal routing line.

Claim 3 (previously presented): The PLD of claim 1, wherein:

for a second set of signal routing lines, each signal routing line in the second set having a partial signal routing line formed from the interface region along that signal routing line,

the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 4 (original): The PLD of claim 3, wherein:

the interface region includes signal lines provided from outside the LE array; and

the signal lines provided from outside the LE array are coupled to at least some of the second set of signal routing lines.

Claim 5 (original): The PLD of claim 3, wherein:

the interface region includes signal lines provided from IP core logic inserted into the LE array; and

the signal lines provided from the IP core logic are coupled to at least some of the second set of signal routing lines via signal selection circuitry.

Claim 6 (previously presented): A programmable logic device (PLD), comprising:

a plurality of logic elements (LE's) arranged in an array;

a signal routing architecture including a plurality of signal routing lines to route signals among the LE's; and

a plurality of signal drivers along each of the signal routing lines,

wherein,

for each of the signal routing lines,

the drivers along that signal routing line are spaced along that signal routing line; and

for each of a first set of at least some of the signal routing lines,

that signal routing line is substantially interrupted by an interface region such that a partial signal routing line is formed for that signal routing line between the interface region and a driver along the signal routing line from the interface region and wherein:

for a second set of signal routing lines, each signal routing line in the second set having a partial signal routing line formed from the interface region along that signal routing line,

the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 7 (cancelled)

Claim 8 (previously presented): The PLD of claim 6, wherein:

the interface region includes signal lines coupled to outside the LE array; and

the signal lines coupled to outside the LE array are coupled to at least some of the second set of signal routing lines.

Claim 9 (previously presented): The PLD of claim 6, wherein:

the interface region includes signal lines coupled to IP core logic inserted into the LE array; and

the signal lines coupled to the IP core logic are coupled to at least some of the second set of signal routing lines via signal selection circuitry.

Claim 10 (previously presented): A programmable logic device (PLD), comprising:

a plurality of logic elements (LE's) arranged in an array;

a signal routing architecture including a plurality of signal routing lines; and

a plurality of signal drivers along each of the signal routing lines,

wherein,

for each of a set of the signal routing lines,

the drivers along that signal routing line are spaced along that signal routing line; and

the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 11 (previously presented): The PLD of claim 10, wherein the signal routing lines of the set of signal routing lines are substantially interrupted by an interface region such that a partial signal routing line is formed for each of at least some of the signal routing lines, between the interface region and a driver along that signal routing line from the interface region.

Claim 12 (previously presented): A method of configuring a design of a programmable logic device (PLD), comprising:

a) configuring the design such that the PLD includes a plurality of logic elements (LE's) arranged in an array;

b) configuring the design such that the PLD includes a signal routing architecture including a plurality of signal routing lines to route signals among the LE's; and

c) configuring the design such that the PLD includes a plurality of signal drivers along each of the signal routing lines,

including,

for each of the signal routing lines,

configuring the design such that the drivers of the PLD along that signal routing line are spaced along that signal routing line; and

for each of a first set of at least some of the signal routing lines,

configuring the design such that the signal routing line of the PLD is substantially interrupted by an interface region such that a partial signal routing line is formed for that signal routing line between the interface region and a driver along the signal routing line from the interface region; and

configuring the design such that the PLD further comprises an input driver configured to drive from the interface region along the partial signal routing line formed for that signal routing line.

Claim 13 (original): The method of claim 12, wherein:

the method includes configuring the design such that, for each of the first set of at least some of the signal routing lines, the input driver configured to drive from the interface region along the partial signal routing lines for that signal routing line is characterized by a size that corresponds to a distance from the interface driver to the driver on the signal routing line closest to the interface region along the signal routing line.

Claim 14 (previously presented): The method of claim 12, wherein:

the method includes configuring the design such that, for a second set of signal routing lines, each signal routing line in the second set and having a partial signal routing line formed from the interface region along that signal routing line, and

the method includes configuring the design such that the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 15 (original): The method of claim 14, wherein:

the method includes configuring the design such that the interface region includes signal lines provided from outside the LE array; and

the method includes configuring the design such that the signal lines provided from outside the LE array are coupled to at least some of the second set of signal routing lines.

Claim 16 (original): The method of claim 14, wherein:

the method includes configuring the design such that the interface region includes signal lines provided from IP core logic inserted into the LE array; and

the method includes configuring the design such that the signal lines provided from the IP core logic are coupled to at least some of the second set of signal routing lines via signal selection circuitry.

Claim 17 (previously presented): A method of configuring a design of a programmable logic device (PLD), comprising:

configuring the design such that the PLD includes a plurality of logic elements (LE's) arranged in an array;

configuring the design such that the PLD includes a signal routing architecture including a plurality of signal routing lines to route signals among the LE's; and

a plurality of signal drivers along each of the signal routing lines,

wherein,

for each of the signal routing lines,

the method includes configuring the design such that the drivers along that signal routing line are spaced along that signal routing line;

for each of a first set of at least some of the signal routing lines,

the method includes configuring the design such that that signal routing line is substantially interrupted by an interface region such that a partial signal routing line is formed for that signal routing line between the interface region and a driver along the signal routing line from the interface region.

and wherein:

the method includes configuring the design such that, for a second set of signal routing lines, each signal routing line in the second set having a partial signal routing line formed from the interface region along that signal routing line,

the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 18 (cancelled)

Claim 19 (previously presented): The method of claim 17, wherein:

the method includes configuring the design such that the interface region includes signal lines coupled to outside the LE array; and

the method includes configuring the design such that the signal lines coupled to outside the LE array are coupled to at least some of the second set of signal routing lines.

Claim 20 (currently amended): The method of claim 17 ~~claim 18~~, wherein:

the method includes configuring the design such that the interface region includes signal lines coupled to IP core logic inserted into the LE array; and

the method includes configuring the design such that the signal lines coupled to the IP core are coupled to at least some of the second set of signal routing lines via signal selection circuitry.

Claim 21 (previously presented): A method of configuring the design of a programmable logic device (PLD), comprising:

configuring the design such that the PLD includes a plurality of logic elements (LE's) arranged in an array;

configuring the design such that the PLD includes a signal routing architecture including a plurality of signal routing lines; and

configuring the design such that a plurality of signal drivers along each of the signal routing lines,

wherein,

the method includes configuring the design such that, for each of a set of the signal routing lines,

the drivers along that signal routing line are spaced along that signal routing line; and

the drivers along each signal routing line of the set are staggered with respect to the drivers along an adjacent signal routing line of the set.

Claim 22 (previously presented): The method of claim 21, wherein the method includes configuring the design such that the signal routing lines of the set of signal routing lines are substantially interrupted by an interface region such that a partial signal routing line is formed for each of at least some of the signal routing lines, between the interface region and a driver along that signal routing line from the interface region.